JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

Course Structure and Syllabus for M.Tech. Embedded Systems
for affiliated Engineering Colleges, 2009-10

I YEAR I SEMESTER

Subject	Hours/ Week
Micro Controllers & Interfacing	4
Operating Systems	4
Embedded System Concepts	4
Advanced Computer Architecture	4
Advanced DSP	4
ELECTIVE I a. Digital IC Design b. VLSI Technology c. Algorithms for VLSI Design Automation	4
LABORATORY: Microcontrollers & Interfacing Lab	4

I YEAR II SEMESTER

Subject	Hours/ Week
Real Time Operating Systems	4
Testing & Testability	4
Hardware Software Co-design	4
FPGA Architecture & Applications	4
Cryptography & Network Security	4
ELECTIVE II a. Radio Frequency Identification b. Micro Electromechanical Systems c. Expert Systems	4
LABORATORY: RTOS & FPGA Lab	4

II YEAR (III & IV Semesters)

SUBJECTS
Seminar
Project work

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
I SEMESTER

MICROCONTROLLERS & INTERFACING

UNIT I
INTEL 8051: Architecture of 8051, Memory Organization, Register banks, Bit addressing media, SFR area, addressing modes, Instruction set, Programming examples.

UNIT II
8051 Interrupt structure, Timer modules, Serial Features, Port structure, Power saving modes.

UNIT III
MOTOROLA 68HC11: Controllers features, Different modes of operation and memory map, Functions of I/O ports in single chip and expanded multiplexed mode, Timer system.

UNIT IV
Input capture, Output compare and pulsed accumulator features of 68HC11, Serial peripherals, Serial Communication interface, Analog to digital conversion features.

UNIT V
PIC MICROCONTROLLERS: Program memory, CPU registers, Register file structure, Block diagram of PIC 16C74, I/O ports. Timer 0,1 and 2 features, Interrupt logic, serial peripheral interface, I^2C bus, ADC, UART, PIC family parts.

UNIT VI
MICROCONTROLLER INTERFACING: 8051, 68HC11, PIC-16C6X and ATMEL External Memory Interfacing – Memory Management Unit, Instruction and data cache, memory controller. On Chip Counters, Timers, Serial I/O, Interrupts and their use. PWM, Watch dog, ISP, IAP features.

UNIT VII
INTERRUPT SYNCHRONIZATION: Interrupt vectors & priority, external interrupt design. Serial I/O DevicesRS232 Specifications, RS422/Apple Talk/ RS 423/RS435 & other communication protocols. Serial Communication Controller.

UNIT VIII
CASE STUDIES: Design of Embedded Systems using the micro controller 8051/ARM6TDMI, for applications in the area of Communications, Automotives, industrial control.

TEXT BOOKS:

1. M.A. Mazadi & J.G. Mazidi, "The 8051 Micro Controller & Embedded Systems", Pearson Education. Asia (2000).
2. John B. Peatman, Designing with PIC Micro Controllers, Pearson Education.
3. Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 1999.

REFERENCES:

1. 8-bit Embedded Controllers, INTEL Corporation 1990.
2. John B.Peatman, "Designing with PIC Microcontrollers", Pearson Education Inc, India, 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
I SEMESTER

OPERATING SYSTEMS

UNIT I
INTRODUCTION: Operating system definition, Objective and functions, types, different parts, Structure of operating system, trends- parallel computing, distributed computing; Open systems, Hardware, software, firmware

UNIT II
PROCESS SCHEDULING: Definition of a process; process states, transitions, process control, suspend and process, interrupt processing, nucleus of an operating system; parallel processing; Mutual exclusion, Critical Section; Solution of mutual exclusion; Semaphores; Deadlock-occurrence, prevention, detection and recovery;

UNIT III
STORAGE MANAGEMENT: Storage organization, management strategies, hierarchy; virtual storage, paging, segmentation.

UNIT IV
FILE SYSTEM MANAGEMENT: File system (function of a file system)- data hierarchy, blocking and buffering, file organization, queued and basic access methods, backup and recovery;

UNIT V
I/O MANAGEMENT: (functions of I/O management subsystem), Distributed computing- OSI view, OSI network management, MAP, TOP, GOSIP, TCP/IP;

UNIT VI
OS SECURITY: Requirements, external security, operational security, surveillance, threat monitoring; Introduction to Cryptography.

UNIT VII &VIII
CASE STUDIES: UNIX- Shell, Kernel, File System, Process Management, Memory Management, I/O System, Distributed UNIX; Example of operating system-MS-DOS, Windows, OS/2, Apple Macintosh & Linux.

TEXT BOOKS:
1. Dietal H.M , "An Introduction to OS" Pearson Education pvt.Ltd/PHI New Delhi, 12th Indian Reprint 2003.
2. Andrew S.Tanenbaum, "Modern OS"PHI Pearson Education pvt.Ltd New Delhi, 3rd Indian Reprint 2004.
3. Silberschatz . A, Galvin.p and Gagne.G, "Operating System Concepts", John Wiley and Sons. Singapore,2002.

REFERENCES:
1. William Stallings, "Operating Systems", Pearson Education pvt.Ltd.
2. D.M. Dhamdhere,"Operating Systems – A Concept Approach", Tata McGraw Hill, 2003.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. (EMBEDDED SYSTEM)

I SEMESTER

EMBEDDED SYSTEM CONCEPTS

UNITI

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

UNIT II

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT III

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

UNIT IV

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT V

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

UNIT VI

INSTRUCTION SETS; Introduction, preliminaries, ARM processor, SHARC processor.

UNIT VII

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications, system analysis and architecture design

UNIT VIII

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes.

TEXT BOOKS:

1. Computers as a component: principles of embedded computing system design- wayne wolf
2. An embedded software premier: David E. Simon
3. Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1. Embedded real time systems programming-sri ram V Iyer, pankaj gupta, TMH, 2004
2. Embedded system design- A unified hardware/software introduction- frank vahid, tony D.Givargis, John Willey, 2002

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. (EMBEDDED SYSTEMS)

I SEMESTER

ADVANCED COMPUTER ARCHITECTURE

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Technology trends, cost- measuring and reporting performance quantitative principles of computer design.

UNIT II

INSTRUCTION SET PRINCIPLES AND EXAMPLES: classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set- instructions for control flow- encoding an instruction set.-the role of compiler

UNIT III

INSTRUCTION LEVEL PARALLELISM (ILP): over coming data hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP

UNIT IV

ILP SOFTWARE APPROACH: Compiler Techniques, Static Branch Protection, VLIW Approach, H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT V

MEMORY HIERARCHY DESIGN: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

UNIT VI

MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

UNIT VII

STORAGE SYSTEMS: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

UNIT VIII

INTER CONNECTION NETWORKS AND CLUSTERS: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster

TEXT BOOKS:

1. John. Hennessy & David A. Patterson Morgan Kufmann, ”Computer Architecture A quantitative approach”, 3rd edition (An Imprint of Elsevier)

REFERENCES:

1. Kai Hwang and A. Briggs, “Computer Architecture and parallel Processing”, International Edition McGraw-Hill.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, “Advanced Computer Architectures”, Pearson.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. (EMBEDDED SYSTEMS)

I SEMESTER

ADVANCED DSP

UNIT I

LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN: Types of Linear-Phase transfer functions, Simple digital filters, Complementary Transfer Functions, Inverse Systems, System identification, Digital Two-Pairs, Algebraic Stability Test.

UNIT II

DIGITAL FILTER STRUCTURE AND DESIGN: All pass filters, Tunable IIR Digital filter, IIR tapped Cascaded Lattice Structures, FIR Cascaded lattice Structures, Parallel All pass realization of IIR Transfer Functions, State Space Structures, Polyphase Structures, Digital Sine-Cosine generator,

UNIT III

Computational Complexity of Digital filter Structures, Design of IIR filter using pade' approximation, Least square design methods, Design of computationally Efficient FIR Filters.

UNIT IV

DSP ALGORITHMS: Fast DFT algorithms based on Index mapping, Sliding Discrete Fourier transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNIT V& VI

ANALYSIS OF FINITE WORD LENGTH EFFECTS: The Quantization Process and errors, Quantization of fixed-point Numbers, Analysis of Coefficient quantization effects, A/D conversion Noise Analysis, Analysis of Arithmetic Round of errors, Dynamic range scaling, Signal to Noise ratio in Low-order IIR Filters, Low sensitivity Digital filters, Reduction of Product Round off Errors using error feedback, Limit cycle in IIR Digital filters, Round of errors in FFT algorithms.

UNIT VII

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis of Sinusoidal Signals, Spectral Analysis of Nonstationary Signals, Musical Sound Processing, Over Sampling A/D Converter, Over Sampling D/A Converter, Discrete –Time Analytic Signal generation.

UNIT VIII

Current Trends in Digital Signal Processors / DSP Controllers - Architecture - DSP Applications.

TEXT BOOKS:

1. Digital Signal Processing by Sanjit K Mitra, Tata MCgraw Hill Publications
2. Digital Signal Processing Principles, Algorithms,Applications By J G Proakis, D G Manolokis,PHI.
3. Discrete-Time Signal Processing by A V Oppenhiem, R W Schafer , Pearson Education Asia.

REFERENCES:

1. Naim Dahnoun, "Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform", 1st Edition.
2. T.J. Terrel and Lik-Kwan Shark, "Digital Signal Processing-A Student Guide", 1st Edition, MACMILLAN PRESS Ltd.
3. David J Defatta J, Lucas Joseph G & Hodkiss William S, "Digital Signal Processing: A System Design Approach", 1st Edition, John Wiley.
4. Rulph Chassaing, "DSP Applications using 'C' and the TMS320C6X DSK", 1st Edition.
5. Andrew Bateman, Warren Yates, "Digital Signal Processing Design", 1st Edition.
6. John G Proakis, Dimitris G Manolakis, "Introduction to Digital Signal Processing", 1st Edition.
7. Kreig Marven & Gillian Ewers, "A Simple approach to Digital Signal processing", 1st Edition, Wiely Interscience.
8. JAMES H. McClellan, Ronald Schaffer and Mark A. Yoder, "DSP FIRST - A Multimedia Approach", 1st Edition, Prentice Hall.
9. Oppenheim A.V and Schafer R.W, "Digital Signal Processing", 1st Edition, PH.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
I SEMESTER

DIGITAL IC DESIGN
(ELECTIVE I)

UNIT I
CMOS inverters -static and dynamic characteristics.

UNIT II
Static and Dynamic CMOS design- Domino and NORA logic - combinational and sequential circuits.

UNIT III
Method of Logical Effort for transistor sizing -power consumption in CMOS gates- Low power CMOS design.

UNIT IV
Arithmetic circuits in CMOS VLSI - Adders- multipliers- shifter -CMOS memory design - SRAM and DRAM

UNIT V
Bipolar gate Design- BiCMOS logic - static and dynamic behaviour -Delay and power consumption in BiCMOS Logic.

UNIT VI&VII
LAYOUT DESIGN RULES: Need for Design Rules, Mead Conway Design Rules for the Silicon Gate NMOS Process, CMOS Based Design Rules, Simple Layout Examples, Sheet Resistance, Area Capacitance, Wire Capacitance, Drive Large Capacitive Load**.**

UNIT VIII
SUBSYSTEM DESIGN PROCESS: General arrangement of 4-bit Arithmetic Processor, Design of 4-bit shifter, Design of ALU sub-system, Implementing ALU functions with an adder, Carry-look-ahead adders, Multipliers, Serial Parallel multipliers, Pipeline multiplier array, modified Booth's algorithm.

TEXT BOOKS:

1. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", MGH, Second Ed., 1999
2. Jan M Rabaey, "Digital Integrated Circuits - A Design Perspective", Prentice Hall, 1997
3. Eugene D Fabricus, "Introduction to VLSI Design,"McGraw Hill International Edition.1990

REFERENCES:

1. Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2000
2. Neil H E West and Kamran Eshranghian,"Principles of CMOS VLSI Design: A System Perspective", Addision-Wesley 2nd Edition,2002.
3. R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS circuit design, layout, and simulation". New York: IEEE Press, 1998.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
I SEMESTER

VLSI TECHNOLOGY
(ELECTIVE I)

UNIT I
REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi-CMOS) Technology trends and projections.

UNIT II
BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids-Vds relationships, Threshold voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT III
LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

UNIT IV
LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT V
COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network Delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT VI
SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT VII
FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High level Synthesis, Architecture for Low Power, SOCs and Embedded Cpus, Architecture Testing.

UNIT VIII
INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and Printing; Hardware/Software Co-Design, Chip Design Methodologies- a Simple Design Example.

TEXT BOOKS:
1. K. Eshraghian et . al(3 authors), “Essentials of VLSI Circuits and Systems”, PHI of India Ltd., 2005
2. Wayne Wolf , “Modern VLSI Design”, 3/E, Pearson Education, fifth Indian Reprint, 2005.

REFERENCES:
1. N.H.E Weste, K.Eshraghian, “Principals of CMOS Design”, Adison Wesley, 2nd Edition.
2. Fabricius, ”Introduction to VLSI Design”, MGH International Edition, 1990.
3. Baker, Li Boyce, “CMOS Circuit Design, Layout and Simulation”, PHI, 2004.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
I SEMESTER

ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE I)

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

UNIT IV

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT V

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

UNIT VI

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT VII

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT VIII

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", Wiley Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd edition, Springer International Edition, 2005.

REFERENCES:

1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley, 1993.
2. Wayne Wolf, "Modern VLSI Design: Systems on silicon", Pearson Education Asia, 2nd Edition, 1998

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. (EMBEDDED SYSTEMS)

I SEMESTER

MICROCONTROLLERS & INTERFACING LAB

ASSEMBLY:

1. Write a program to a) Clear the Register and b) Add 3 to Register Ten Times and Place the Result into Memory Use the Indirect Instructions to Perform Looping.

PROGRAMING IN C:

2. A Door Sensor is connected to RB1 Pin and a Buzzer is connected to RB7. Write a Program to monitor Door Sensor and when it Open, Sounds the Buzzer by sending a Square Wave of few Hundred Hz Frequency to it.

3. Write a Program to Toggle all the Bits of PORT B parts continuously with a 250ns Delay.

4. Stepper Motor Control using Microcontroller.

Use Microcontrollers for the following Experiments.

INTERFACING:

5. Elevator Interface.
6. Key Board Interface.
7. LED Interface.
8. Temperature Sensor.
9. SORT RTO'S on to 89c51 Board.
10. Sample the Signal using ADC and Reconstruct by using DAC.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
II SEMESTER

REAL TIME OPERATING SYSTEMS

UNIT I

INTRODUCTION TO UNIX: Overview Of Commands, File I/O. (Open, Create, Close, Lseek, Read, Write), Process Control (Fork, Vfork, Exit, Wait, Waitpid, Exec), Signals, Inter Process Communication (Pipes, FIFOs, Message Queues, Semaphores, Shared Memory).

UNIT II&III

REAL TIME SYSTEMS: Typical Real Time Application, Hard Vs Soft Real Time Systems, a Reference Model of Real Time Systems: Processors and Resources, Temporal Parameters of Real Time Workload, Periodic Task Model, Precedence Constraints and Data Dependency Functional Parameters, Resource Parameters of Jobs and Parameters of Resources

UNIT IV

APPROACHES TO REAL TIME SCHEDULING: Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective Release Times and Dead Lines, Offline Vs Online Scheduling.

UNIT V

OPERATING SYSTEMS: Overview, Time Services and Scheduling Mechanisms, other Basic Operating System Function, Processor Reserves and Resource Kernel. Capabilities of Commercial Real Time Operating Systems.

UNIT VI

FAULT TOLERANCE TECHNIQUES: Introduction, Fault Causes, Types, Detection, Fault and Error Containment, Redundancy: Hardware, Software, Time. Integrated Failure Handling.

UNIT VII

CASE STUDIES-VX WORKS: Memory Managements Task State Transition Diagram, Pre-Emptive Priority, Scheduling, Context Switches – Semaphore – Binary Mutex, Counting: Watch Dugs, I/O System

UNIT VIII

RT Linux: Process Management, Scheduling, Interrupt Management, and Synchronization

TEXT BOOKS:

1. Richard Stevens, “Advanced Unix Programming”.
2. Jane W.S. Liu, “Real Time Systems”, Pearson Education.
3. C.M.Krishna, KANG G. Shin, “Real Time Systems”, McGraw.Hill

REFERENCES:

1. VxWorks Programmers Guide
2. www.tidp.org
3. www.kernel.org
4. http://www.xml.com/ldd/chapter/book

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
II SEMESTER

TESTING & TESTABILITY

UNIT I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation.

UNIT II

FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits.

UNIT III

TESTING FOR SINGLE STUCK FAULTS (SSF): Automated Test Pattern Generation (ATPG/ATG) For Ssfs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models. Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

UNIT IV&V

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques. Scan Architectures and Testing – Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards. Compression Techniques – Different Techniques, Syndrome Test and Signature Analysis.

UNIT VI

BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT VII

MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

UNIT VIII

BRIEF IDEAS ON EMBEDDED CORE TESTING: Introduction to Automatic in Circuit Testing (ICT), JTAG Testing Features.

TEXT BOOKS:

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.

REFERENCES:

1. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
2. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
II SEMESTER

HARDWARE SOFTWARE CO- DESIGN

UNIT I

CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

UNIT II

CO- SYNTHESIS ALGORITHMS: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT III

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

UNIT IV

TARGET ARCHITECTURES: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT V

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT VI

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT VII

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages,

UNIT VIII

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, “Hardware / software co- design Principles and Practice”, Springer, 2009.
2. Kluwer, “Hardware / software co- design Principles and Practice”, academic publishers,2002.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
II SEMESTER

FPGA ARCHITECTURE & APPLICATIONS

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

FPGA: Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

UNIT III

CASE STUDIES: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

UNIT IV

FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT V

REALIZATION OF STATE MACHINE: Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT VI& VII

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT VIII

DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

TEXT BOOKS/ REFERENCES:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, jPrentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publicatgions,1994.

3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
II SEMESTER

CRYPTOGRAPHY & NETWORK SECURITY

UNIT I

SYMMETRIC CIPHERS: Overview, classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

UNIT II

PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS: Introduction to Number Theory, Public-Key Cryptography and RSA-Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT III

NETWORK SECURITY PRACTICE: Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

UNIT IV

SYSTEM SECURITY: Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

UNIT V

WIRELESS SECURITY: Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

UNIT VI

SECURE NETWORKING THREATS: Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

UNIT VII

ENCRYPTION TECHNIQUES: Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

UNIT VIII

DESIGNING SECURE NETWORKS: Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, The Difficulties of Secure Networking, Security Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security Considerations, IP Addressing Design Considerations, ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security – Principles And Practices", Pearson Education, 3rd Edition, 2003.
2. Sean Convery, " Network Security Architectures, Published by Cisco Press, First Ed. 2004.

REFERENCES:

1. Atul Kahate, "Cryptography and Network Security", Tata McGraw Hill, 2003.
2. Bruce Schneier, "Applied Cryptography", John Wiley and Sons Inc, 2001.
3. Stewart S. Miller, "Wi-Fi Security", McGraw Hill, 2003.
4. Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security In Computing", 3rd Edition, Pearson Education, 2003.
5. Jeff Crume, "Inside Internet Security" Addison Wesley, 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
II SEMESTER

RADIO FREQUENCY IDENTIFICATION
(ELECTIVE II)

UNIT I

UNDERSTANDING RFID TECHNOLOGY: Introduction, RFID Technology, The Elements of an RFID system, Coupling, Range, and Penetration, RFID Applications, VeriChip and Mark of the Beast.

UNIT II&III

A HISTORY OF THE EPC: Introduction, The Distributed Intelligent Systems Center, Meanwhile, at Procter & Gamble, "Low-Cost" RFID Protocols, "Low-cost" Manufacturing, The Software and the Network, Privacy, Harnessing the Juggernaut, The Six Auto-ID Labs, The Evolution of the Industry, The Creation of EPC global.

UNIT IV&V

RFID AND GLOBAL PRIVACY POLICY: Introduction, Definitions of Privacy, Definitions of Personal Information, History of Current Privacy Paradigm, Mapping the RFID Discovery process, Functions and Responsibilities for chips, Readers, and Owners, Privacy as a Fundamental Human Right, Constitutional Rights.

UNIT VI&VII

RFID, PRIVACY, AND REGULATION: Introduction, Understanding RFID's Privacy Threats. RFID and the United States Regulatory Landscape: Introduction, Current State of RFID Policy, Individuals, Business, Government, Miscellaneous, Integrity and Security of the System, Government Access, Health Impact, Labor Impact

UNIT VIII

APPLICATIONS: RFID Payments at ExxonMobil, Exxon Mobil Corporation, Transforming the Battlefield with RFID, Logistics and the Military, RFID in the Pharmacy, CVS and Auto-ID, Project Jump Start, RFID in the Store.

TEXT BOOKS:

1. Simson Garfinkel and Beth Rosenberg, "RFID Applications, Security, and privacy", Pearson Education
2. Steven Shepard, "Radio Frequency Identification", First edition, McGraw-Hill Professional.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
II SEMESTER

MICRO ELECTROMECHANICAL SYSTEMS
(ELECTIVE II)

UNIT I&II

INTRODUCTION, BASIC STRUCTURES OF MEM DEVICES: (Canti Levers, Fixed Beams diaphragms). Broad Response of Micro Electromechanical Systems (MEMs) to Mechanical (force, pressure etc.) Thermal, Electrical, Optical and Magnetic stimuli, Compatability of MEMS from the point of Power Dissipation, Leakage etc.

UNIT III

REVIEW OF MECHANICAL CONCEPTS: Stress, Strain, Bending Moment, Deflection Curve. Differential Equations Describing the Deflection under Concentrated Force, Distributed Force, Deflection Curves for Canti Levers – Fixed Beam. Electrostatic Excitation – Columbic Force between the Fixed and Moving Electrodes. Deflection with Voltage in C.L, Deflection Vs Voltage Curve, Critical Fringe Fields – Field Calculations using Laplace Equation. Discussion on the Approximate Solutions – Transient Response of the MEMS.

UNIT IV

TWO TERMINAL MEMS: Capacitance Vs Voltage Curve – Variable Capacitor. Applications of Variable Capacitors. Two Terminal MEM Structures. Three Terminal MEM Structures – Controlled Variable Capacitors – MEM as a Switch and Possible Applications.

UNIT V&VI

MEM CIRCUITS & STRUCTURES FOR SIMPLE GATES: AND, OR, NAND, NOR, Exclusive OR, simple MEM Configurations for Flip-Flops Triggering, Applications to Counters, Converters. Applications for Analog Circuits like Frequency Converters, Wave Shaping. RF Switches for Modulation. MEM Transducers for Pressure, Force Temperature. Optical MEMS.

UNIT VII&VIII

MEM TECHNOLOGIES: Silicon Based MEMS – Process Flow – Brief Account of Various Processes and Layers like Fixed Layer, Moving Layers, Spacers Etc., Etching Technologies. Metal Based MEMS: Thin and Thick Film Technologies for MEMS. PROCESS flow and Description of the Processes. Status of MEMS in the Current Electronics scenario.

TEXT BOOKS:

1. Gabriel.M.Review, "R.F. MEMS Theory, Design and Technology", John Wiley & Sons, 2003.
2. Thimo Shenko, "Strength of Materials", CBS Publishers & Distributors., 2000.
3. Ristic L. (Ed.), "Sensor Technology and Devices", Artech House, London 1994.
4. Servey E.Lyshevski, "MEMS and NEMS, Systems Devices; and Structures", CRC Press, 2002.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
M.Tech. (EMBEDDED SYSTEMS)
II SEMESTER

EXPERT SYSTEMS
(ELECTIVE II)

UNIT I

KNOWLEDGE REPRESENTATION AND ISSUES: Notational systems: Trees, graphs, hierarchies, propositional and predicate logics, frames, semantics networks, constraints, conceptual dependencies, database, knowledge discovery in databases (KDD).

UNIT II

SEARCH: State-space representations, Depth-first, breadth-first, heuristic search, Planning and game playing, Genetic algorithms.

UNIT III&IV

LOGICAL REASONING AND PROBABILISTIC REASONING: Predicate, Calculus resolution, completeness, and strategies, Unification, Prolog, monotonic and non-monotonic reasoning, Probabilistic inference networks, Fuzzy inference rules, Bayesian rules. Dempster-Shafer Calculus.

UNIT V&VI

LEARNING AND COMMON SENSANE REASONING: Robot actions, strips, triangle tables, case based reasoning, spatial and temporal formalisms. Knowledge acquisition, classification rules, self directed systems.

UNIT VII&VIII

NEURAL NETWORKS AND EXPERT SYSTEMS: Principles, biological analogies, Training (techniques and errors), Recognition, Expert Systems, Organization, tools, limits, examples.

TEXT BOOKS:

1. Charniak .E,And McDermott .D., ”Intoduction to Artificial intelligence”, Adiison-Wesley, 1987
2. Giarratano.J.,And Riley G., ”Expert Systems principles an Programming” PWS-KENT,1989

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. (EMBEDDED SYSTEMS)

II Semester

RTOS & FPGA Lab

1. RTOS System solution & tools
2. Testing RTOS Environment and System Programming.
   a) Keil Tools
   b) RTOS System Solutions with Tornado tools.
3. Embedded DSP based System Designing.
   a) Code compressor studio (CCS) for embedded DSP using Texas tool kit.
   b) Analog DSP tool kit.
4. Synthesis of the designs made using "VHDL / VERILOG and Mixed Design (VHDL & Verilog)" after Simulation are to be verified using FPGA/CPLD blocks from different commercially available products on:

a). Synthesis of 4 to 6-MSI Digital blocks (Combinational Circuits)

b) Synthesis of Sequential Circuits – 6 to 8 MSI and 1 or 2 VLSI Circuits.

NOTE: Required Software Tools for FPGA:

1. Mentor Graphic tools / Cadance tools/ Synophysis tools. (220 nm Technology and Above)
2. Xilinx 9.1i and Above for FPGA/CPLDS / FPGA Advantage.